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Doc. Number:

☐ Tentative Specification
■ Preliminary Specification
☐ Approval Specification

MODEL NO.: N101ICG
SUFFIX: L11

Customer:
APPROVED BY **SIGNATURE**

Name / Title
Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By

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REVISION HISTORY

Version	Date	Page	Description
0.0	July, 05, 2013	All	Spec Ver.0.0 was first issued.
1.0	July, 11, 2013	All	Spec Ver.1.0 was first issued.

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1. GENERAL DESCRIPTION

1.1 OVERVIEW

N101ICG-L11 is a 10” (10.1” diagonal) TFT Liquid Crystal Display module with LED Backlight unit and 40 pins LVDS interface. This module supports 1280 x 800 WXGA mode.

1.2 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Screen Size	10.1 diagonal		
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1280 x R.G.B. x 800	pixel	-
Pixel Pitch	0.1695 (H) x 0.1695 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	262,144	color	-
Transmissive Mode	Normally black	-	-
Surface Treatment	Hard coating (3H), Anti-Glare	-	-
Luminance, White	350	Cd/m2	
Power Consumption	Total 2.96 W (Max.) @ cell 0.76 W (Max.), BL 2.20 W (Max.)		(1)

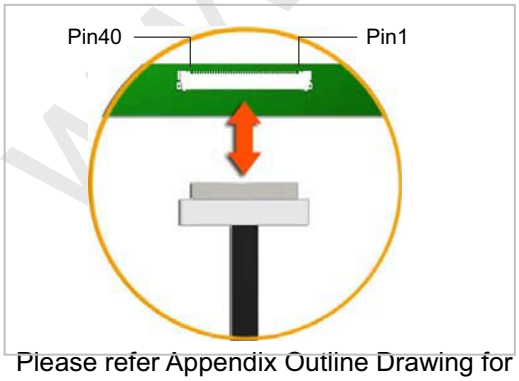
Note (1) The specified power consumption (with converter efficiency) is under the conditions at VCCS = 3.3 V, fv = 60 Hz, LED_VCCS = Typ, fPWM = 200 Hz, Duty=100% and Ta = 25 ± 2 ºC, whereas mosaic pattern is displayed.

2. MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	227.12	227.42	227.72	mm	(1)
	Vertical (V)	147.19	147.69	147.99	mm	
	Thickness (T)	-	2.16(w/o PCBA) 4.36(w/ PCBA)	2.35 4.85	mm	
Bezel Area	Horizontal	219.06	219.31	219.56	mm	
	Vertical	138.0	138.25	138.50	mm	
Active Area	Horizontal	216.66	216.96	217.26	mm	
	Vertical	135.3	135.60	135.9	mm	
Weight		-	120	135	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2.1 CONNECTOR TYPE



Please refer Appendix Outline Drawing for detail design.

Connector Part No.: IPEX-20455-040E-12

User’s connector Part No: IPEX-20453-040T-01

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3. ABSOLUTE MAXIMUM RATINGS

3.1 ABSOLUTE RATINGS OF ENVIRONMENT

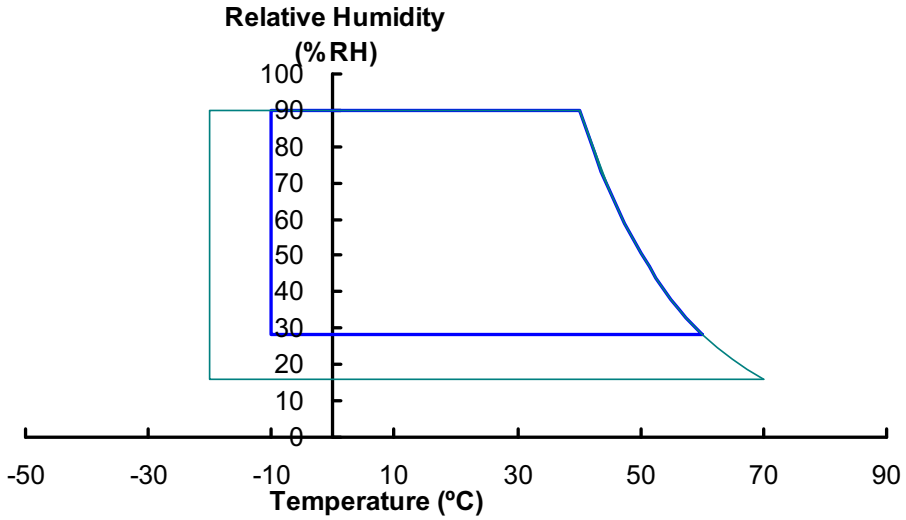
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+70	ºC	(1)
Operating Ambient Temperature	T_{OP}	-10	+60	ºC	(1), (2)

Note (1) (a) 90 %RH Max. (Ta <= 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

(c) No condensation.

Note (2) The temperature of panel surface should be -10 ºC min. and 70 ºC max.



3.2 ELECTRICAL ABSOLUTE RATINGS

3.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCCS	-0.3	+4.0	V	(1)
Logic Input Voltage	V_{IN}	-0.3	VCCS+0.3	V	
Converter Input Voltage	LED_VCCS	-0.3	25	V	(1)
Converter Control Signal Voltage	LED_PWM,	-0.3	5	V	(1)
Converter Control Signal Voltage	LED_EN	-0.3	5	V	(1)

Note (1) Stresses beyond those listed in above “ELECTRICAL ABSOLUTE RATINGS” may cause permanent damage to the device. Normal operation should be restricted to the conditions described in “ELECTRICAL CHARACTERISTICS”.

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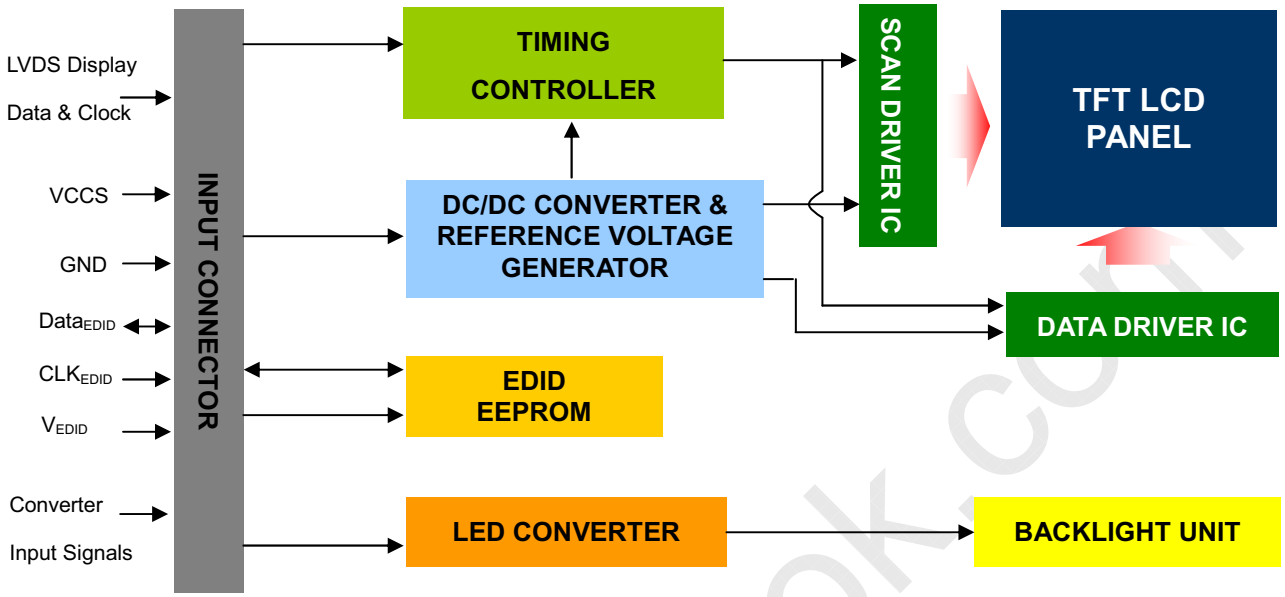
4. ELECTRICAL SPECIFICATIONS

4.1 FUNCTION BLOCK DIAGRAM



4.2. INTERFACE CONNECTIONS

PIN ASSIGNMENT

Pin	Symbol	Description	Remark
1	NC	No Connection (Reserve)	
2	VCCS	Power Supply (3.3V typ.)	
3	VCCS	Power Supply (3.3V typ.)	
4	VEDID	DDC 3.3V power	
5	NC	No Connection (Reserved for CMI test)	
6	CLKEDID	DDC clock	
7	DATAEDID	DDC data	
8	Rxin0-	LVDS differential data input	R0-R5, G0
9	Rxin0+	LVDS differential data input	
10	VSS	Ground	
11	Rxin1-	LVDS differential data input	G1~G5, B0, B1
12	Rxin1+	LVDS differential data input	
13	VSS	Ground	
14	Rxin2-	LVDS Differential Data Input	B2-B5,HS,VS, DE
15	Rxin2+	LVDS Differential Data Input	
16	VSS	Ground	
17	RxCLK-	LVDS differential clock input	LVDS CLK
18	RxCLK+	LVDS differential clock input	
19	VSS	Ground	
20	NC	No Connection (Reserve)	
21	NC	No Connection (Reserve)	
22	VSS	Ground	
23	NC	No Connection (Reserve)	

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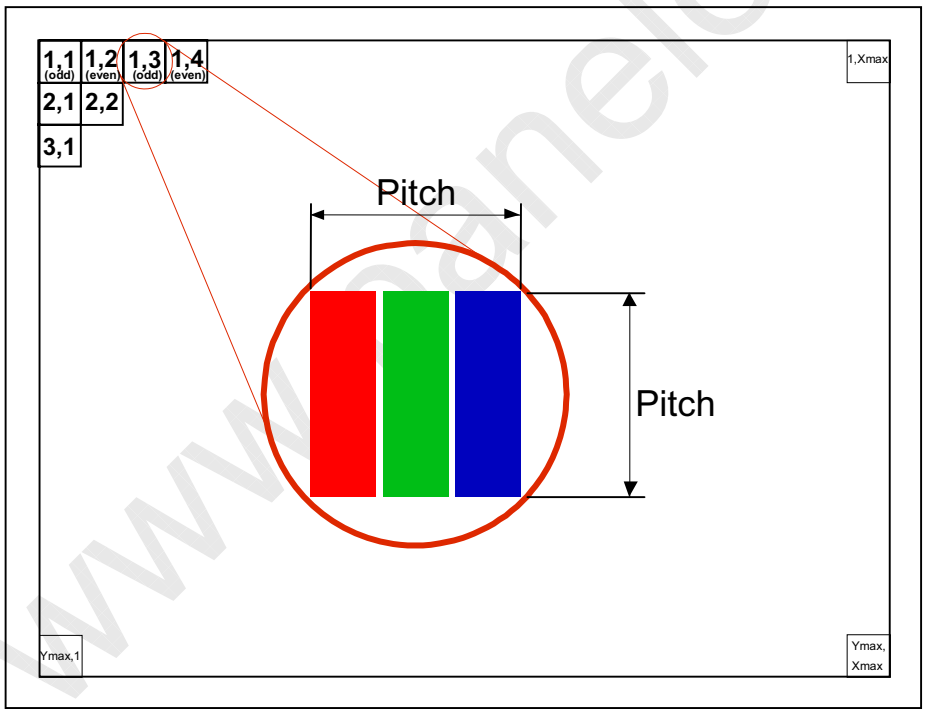
24	NC	No Connection (Reserve)	
25	VSS	Ground	
26	NC	No Connection (Reserve)	
27	NC	No Connection (Reserve)	
28	VSS	Ground	
29	ID1	Connect a 10Kohm to GND	
30	ID2	Connect a 10Kohm to GND	
31	LED_GND	LED Ground	
32	LED_GND	LED Ground	
33	LED_GND	LED Ground	
34	NC	No Connection (Reserve)	
35	LED_PWM	PWM Control Signal of LED Converter	
36	LED_EN	Enable Control Signal of LED Converter	
37	NC	No Connection (Reserve)	
38	LED_VCCS	LED Power Supply	
39	LED_VCCS	LED Power Supply	
40	LED_VCCS	LED Power Supply	

Note (1) The first pixel is odd as shown in the following figure.



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4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD ELETRONICS SPECIFICATION

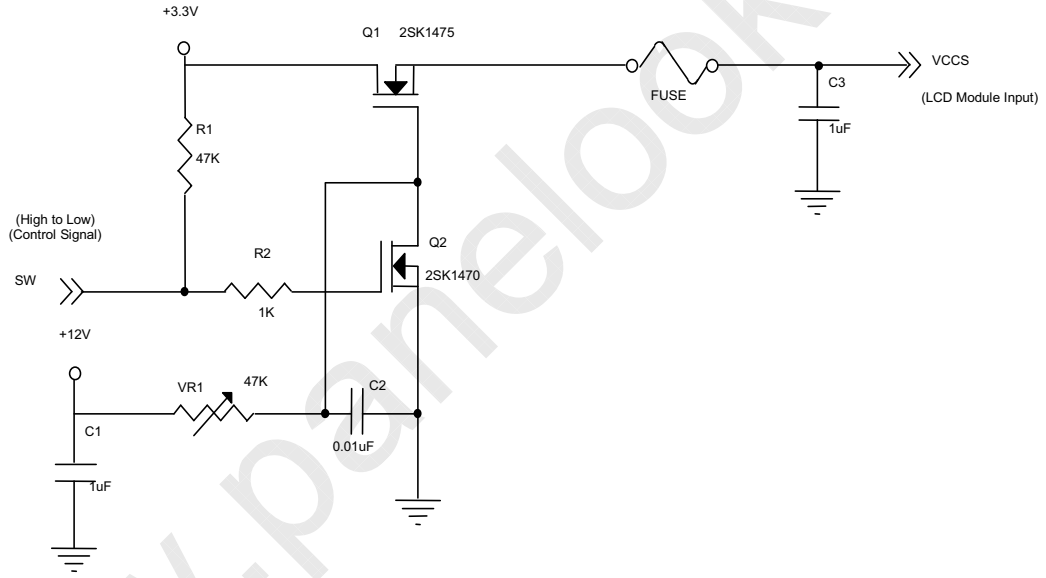
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VCCS	3.0	3.3	3.6	V	(1)-
Ripple Voltage		V_{RP}	-	50	-	mV	(1)-
Inrush Current		I_{RUSH}	-	-	1.5	A	(1),(2)
Power Supply Current	Mosaic	Icc	160	190	230	mA	(3)a
	White		185	220	265	mA	

Note (1) The ambient temperature is Ta = 25 ± 2 ºC.

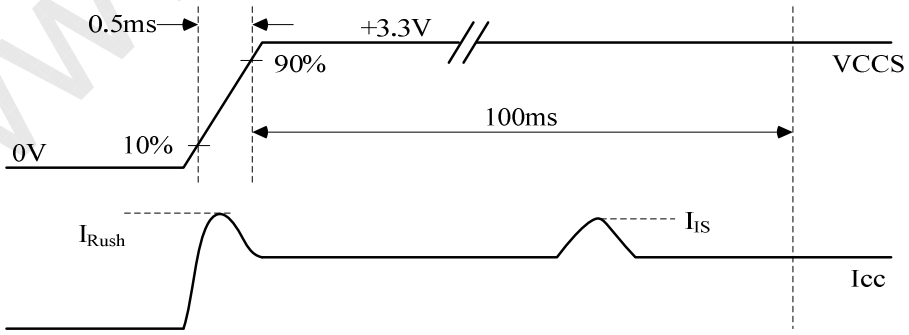
Note (2) I_{RUSH}: the maximum current when VCCS is rising

I_{IS}: the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: white.



VCCS rising time is 0.5ms



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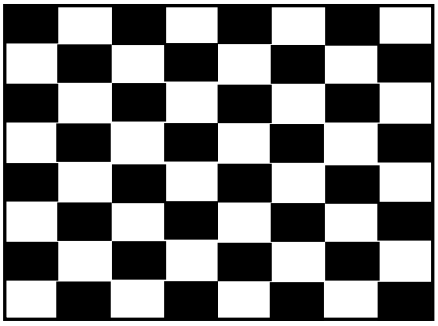
Note (3) The specified power supply current is under the conditions at VCCS = 3.3 V, Ta = 25 ± 2 ºC, DC Current and f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. Mosaic Pattern



Active Area

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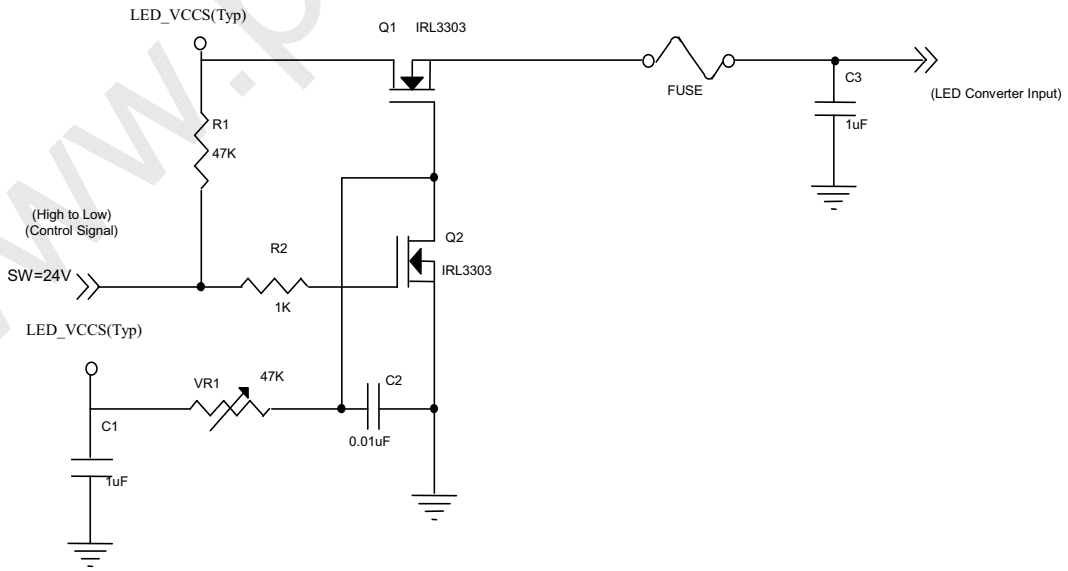
4.3.2 LED CONVERTER SPECIFICATION

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Converter Input power supply voltage		LED_Vccs	3.2	3.7	4.2	V	
Converter Inrush Current		$ILED_{RUSH}$	-	-	1.5	A	(1)
EN Control Level	Backlight On		3.0	-	3.6	V	
	Backlight Off		0	-	0.5	V	
PWM Control Level	PWM High Level		3.0	-	3.6	V	
	PWM Low Level		0	-	0.5	V	
PWM Control Duty Ratio			10	-	100	%	
			5	-	100	%	(2)
PWM Control Permissive Ripple Voltage		VPWM_pp	-	-	100	mV	
PWM Control Frequency		f_{PWM}	190	-	2K	Hz	(3)
LED Power Current	LED_VCCS =Typ.	ILED	450	532	609	mA	(4)

Note (1) $ILED_{RUSH}$: the maximum current when LED_VCCS is rising,

$ILED_{IS}$: the maximum current of the first 100ms after power-on,

Measurement Conditions: Shown as the following figure. LED_VCCS = Typ, Ta = 25 ± 2 ºC, f_{PWM} = 200 Hz, Duty=100%.



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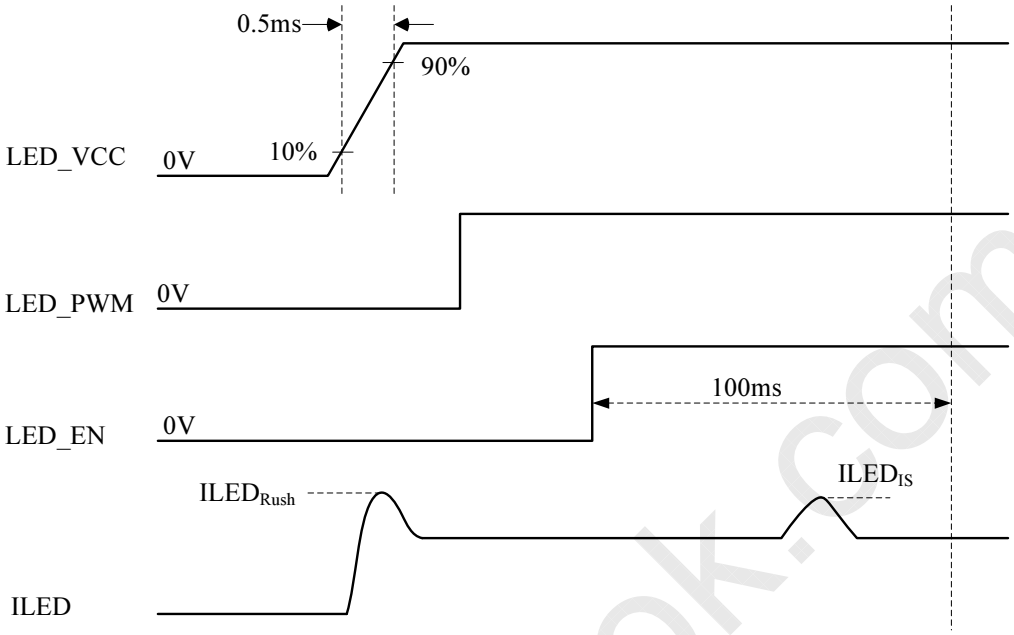
VLED rising time is 0.5ms



Note (2) If the PWM control duty ratio is less than 10%, there is some possibility that acoustic noise or backlight flash can be found. And it is also difficult to control the brightness linearity.

Note (3) If PWM control frequency is applied in the range less than 1KHz, the "waterfall" phenomenon on the screen may be found. To avoid the issue, it's a suggestion that PWM control frequency should follow the criterion as below.

PWM control frequency f_{PWM} should be in the range

$$(N+0.33)*f \leq f_{PWM} \leq (N+0.66)*f$$

N : Integer $(N \geq 3)$

f : Frame rate

Note (4) The specified LED power supply current is under the conditions at "LED_VCCS = Typ.", Ta = 25 ± 2 ºC, f_{PWM} = 200 Hz, Duty=100%.

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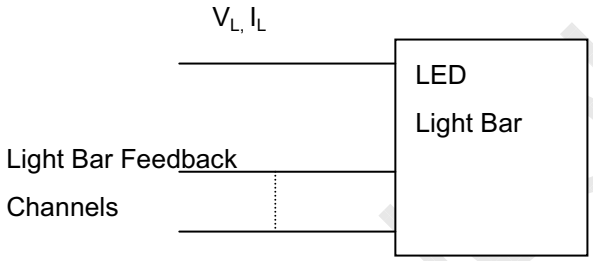
4.3.3 BACKLIGHT UNIT

Ta = 25 ± 2 ºC

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Light Bar Power Supply Voltage	V_L	8.4	9	9.9	V	(1)(2)(Duty100%)
LED Light Bar Power Supply Current	I_L	-	178.4	-	mA	
Power Consumption	P_L	-	1.61	1.77	W	(3)
LED Life Time	L_{BL}	12000	-	-	Hrs	(4)

Note (1) LED current is measured by utilizing a high frequency current meter as shown below :



Note (2) For better LED light bar driving quality, it is recommended to utilize the adaptive boost converter with current balancing function to drive LED light-bar.

Note (3) $P_L = I_L \times V_L$ (Without LED converter transfer efficiency)

Note (4) The lifetime of LED is defined as the time when it continues to operate under the conditions at Ta = 25 ±2 °C and I_L = 20 mA(Per EA) until the brightness becomes ≦ 50% of its original value.

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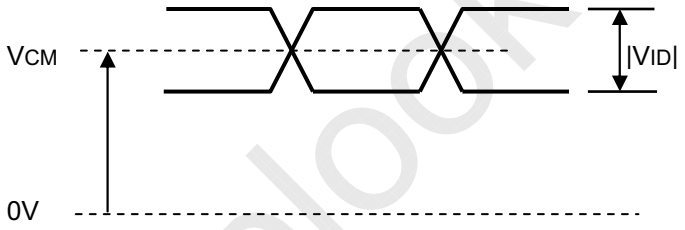
4.4 LVDS INPUT SIGNAL TIMING SPECIFICATIONS

4.4.1 LVDS DC SPECIFICATIONS

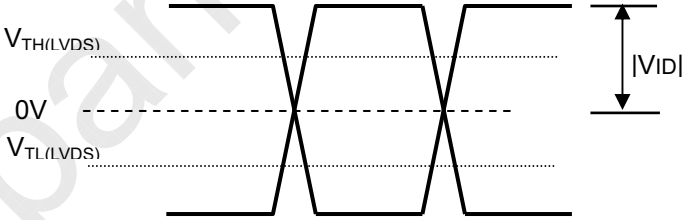
Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LVDS Differential Input High Threshold	$V_{TH(LVDS)}$	-	-	+100	mV	(1), V_{CM}=1.2V
LVDS Differential Input Low Threshold	$V_{TL(LVDS)}$	-100	-	-	mV	(1) V_{CM}=1.2V
LVDS Common Mode Voltage	V_{CM}	1.125	-	1.375	V	(1)
LVDS Differential Input Voltage	$\|V_{ID}\|$	100	-	600	mV	(1)
LVDS Terminating Resistor	R_T	-	100	-	Ohm	-

Note (1) The parameters of LVDS signals are defined as the following figures.

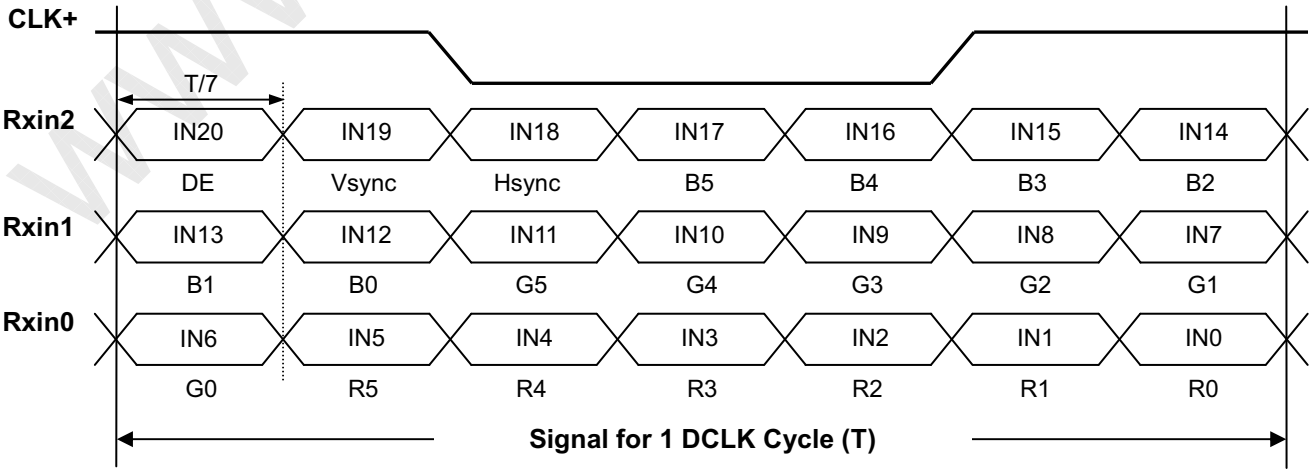
Single Ended



Differential



4.4.2 LVDS DATA FORMAT



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4.4.3 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Basic	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
Colors	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Scale	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Of	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Red	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Gray	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Scale	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Of	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Green	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Gray	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Scale	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Of	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Blue	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

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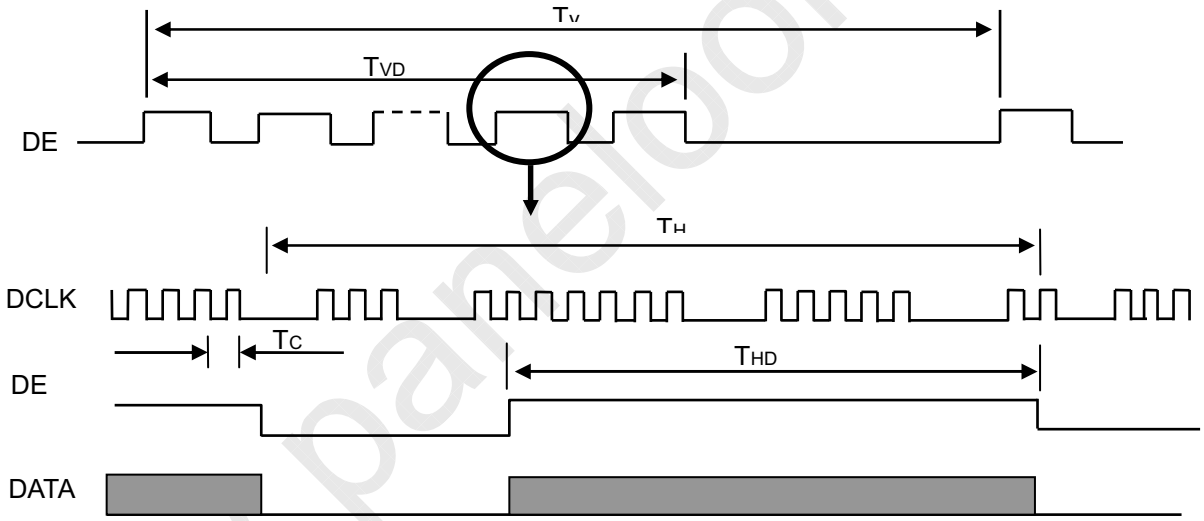
4.5 DISPLAY TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	64	71.1	74.7	MHz	-
DE	Vertical Total Time	TV	810	823	829	TH	-
	Vertical Active Display Period	TVD	800	800	800	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	23	TV-TVD	TH	-
	Horizontal Total Time	TH	1362	1440	1480	Tc	-
	Horizontal Active Display Period	THD	1280	1280	1280	Tc	-
	Horizontal Active Blanking Period	THB	TH-THD	160	TH-THD	Tc	-

Note (1) Because this module is operated by DE only mode, Hsync and Vsync are ignored.

INPUT SIGNAL TIMING DIAGRAM



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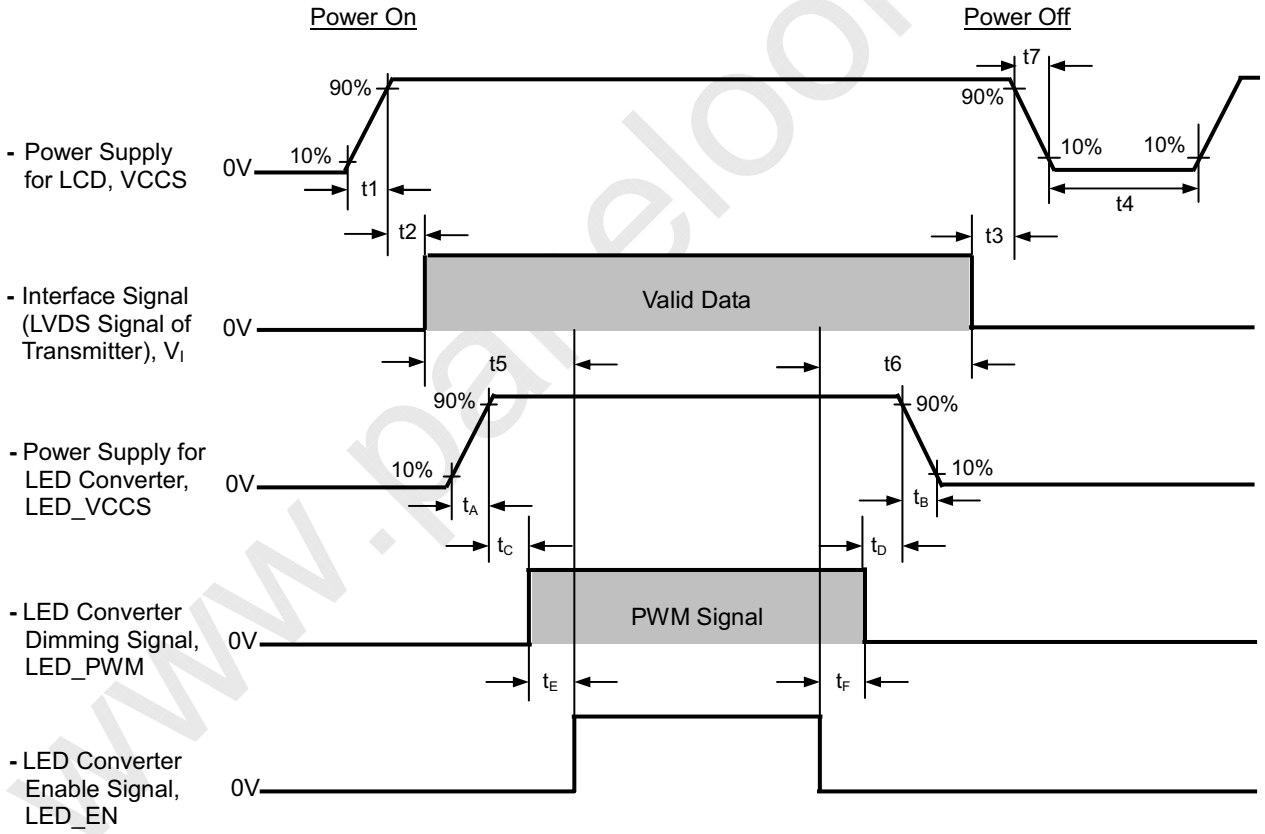
4.6 POWER ON/OFF SEQUENCE

The power sequence specifications are shown as the following table and diagram.

Symbol	Value			Unit	Note
	Min.	Typ.	Max.		
t1	0.5	-	10	ms	
t2	0	-	50	ms	
t3	0	-	50	ms	
t4	500	-	-	ms	
t5	200	-	-	ms	
t6	200	-	-	ms	
t7	0.5	-	10	ms	
t_A	0.5	-	10	ms	
t_B	0		10	ms	
t_C	10	-	-	ms	
t_D	10	-	-	ms	
t_E	10	-	-	ms	
t_F	10	-	-	ms	



Note (1) Please don't plug or unplug the interface cable when system is turned on.

Note (2) Please avoid floating state of the interface signal during signal invalid period.

Note (3) It is recommended that the backlight power must be turned on after the power supply for LCD and the interface signal is valid.

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5. OPTICAL CHARACTERISTICS

5.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Light Bar Input Current	I_L	178.4	mA

The measurement methods of optical characteristics are shown in Section 5.2. The following items should be measured under the test conditions described in Section 5.1 and stable environment shown in Note (5).

5.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing Normal Angle	500	700	-	-	(2), (5) ,(7)
Response Time		T_R		-	14	17	ms	(3) ,(7)
		T_F		-	11	14	ms	
Cross Talk		CT		-	-	4	%	(8)
Average Luminance of White		L_{AVE}		300	350	-	cd/m^2	(4), (6) ,(7)
Color Chromaticity	Red	Rx		Typ – 0.03	0.592	Typ + 0.03	-	(1) ,(7)
		Ry			0.340		-	
	Green	Gx			0.310		-	
		Gy			0.579		-	
	Blue	Bx			0.150		-	
		By			0.128		-	
	White	Wx			0.308		-	
		Wy			0.324		-	
Color Gamut		CG		47	50		%	(9)
Viewing Angle	Horizontal	θ_x+	CR≥10	80	85		Deg.	(1),(5) , (7)
		θ_x-		80	85	-		
	Vertical	θ_Y+		80	85	-		
		θ_Y-		80	85	-		
White Variation of 5 Points		δW_{5p}	θ_x=0°, θ_Y =0°	80	90	-	%	(5),(6) , (7)

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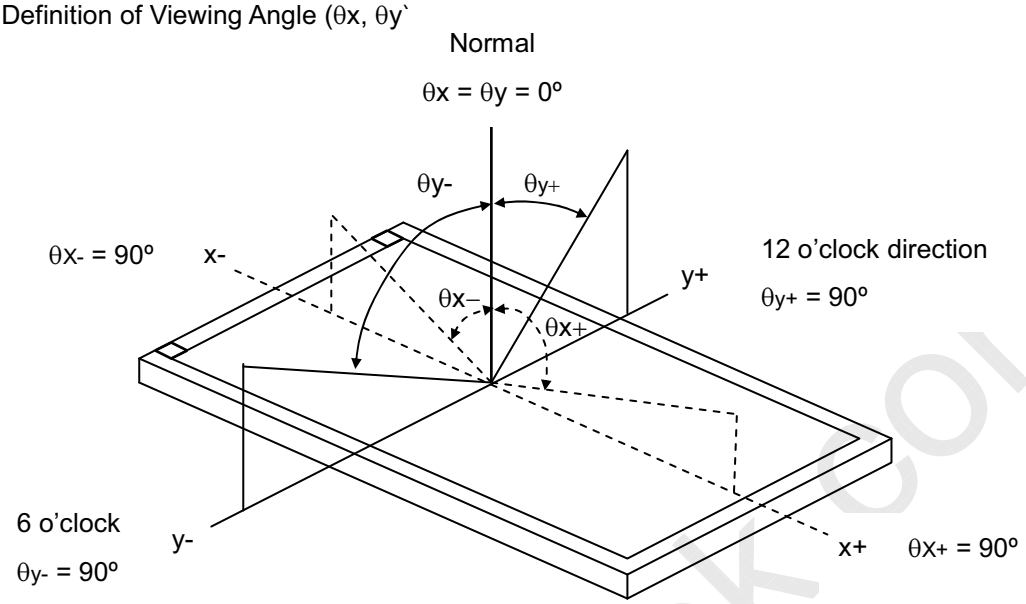
Note (1) Definition of Viewing Angle (θx, θy`



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L63 / L0

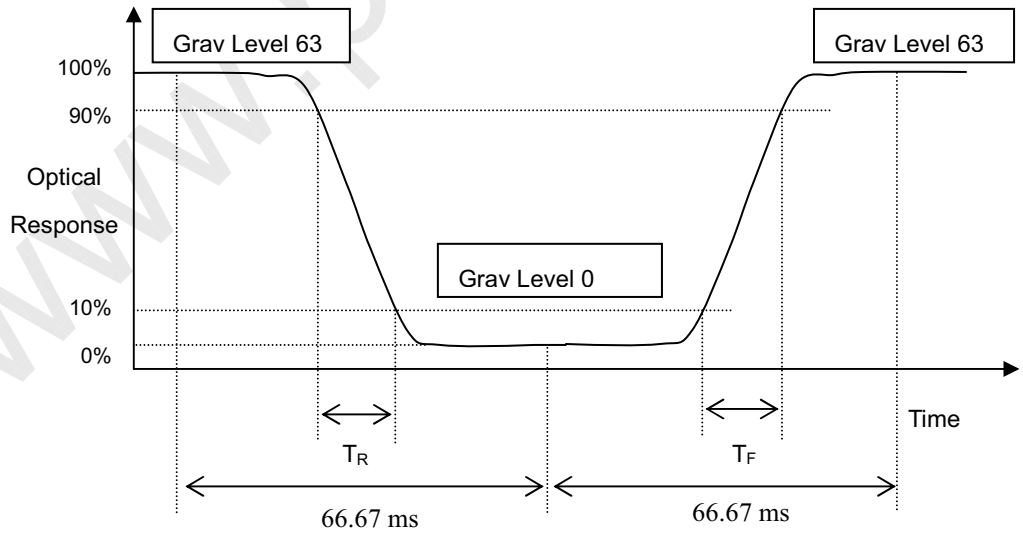
L63: Luminance of gray level 63

L 0: Luminance of gray level 0

CR = CR (1)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R, T_F):



Note (4) Definition of Average Luminance of White (L_{AVE}):

Measure the luminance of gray level 63 at 5 points

L_{AVE} = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5

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L (x) is corresponding to the luminance of the point X at Figure in Note (6)

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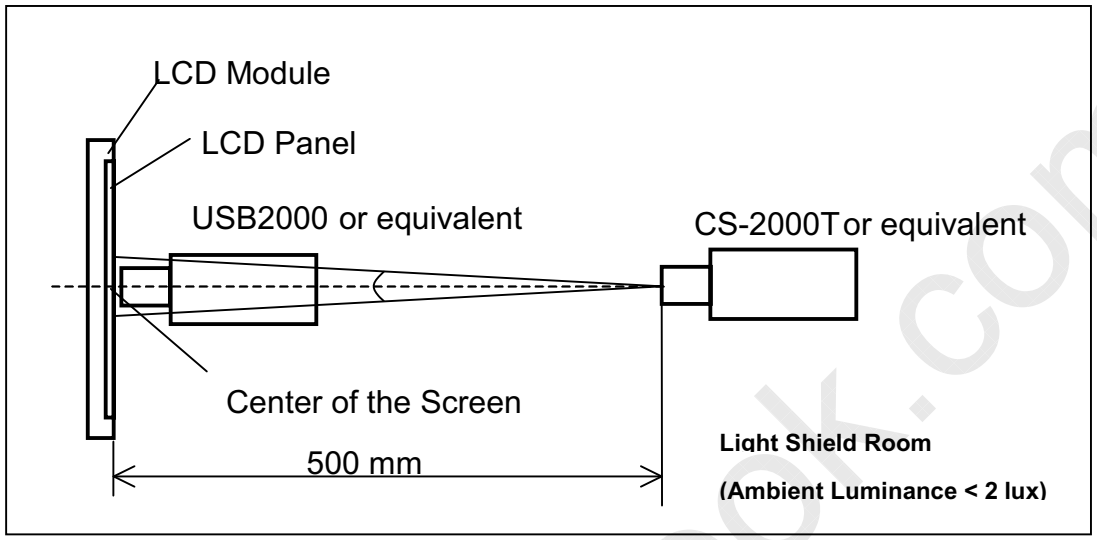
Note (5) Measurement Setup:

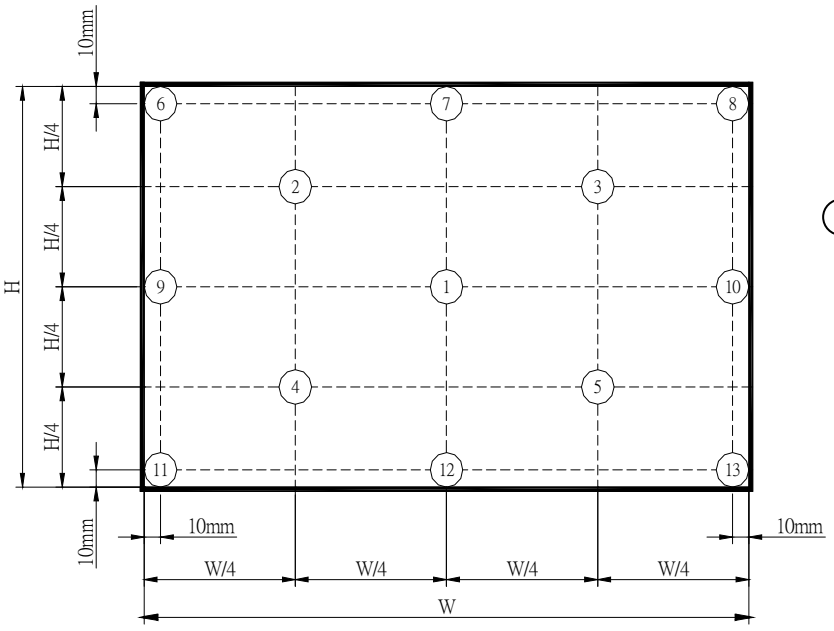
The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 63 at 5 points

δW_{5p} = {Minimum [L (1) ~ L (5)] / Maximum [L (1) ~ L (5)]}*100%



X : Test Point

X=1 to 13

Active area

Note (7) The listed optical specifications refer to the initial value of manufacture, but the condition of the specifications after long-term operation will not be warranted.

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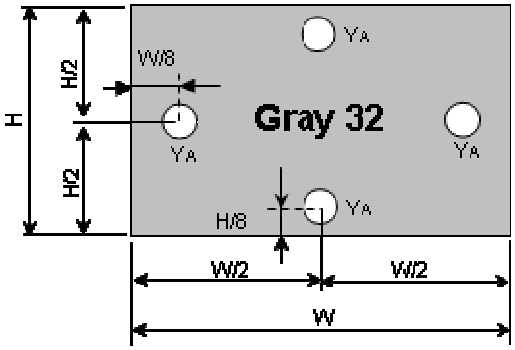
Note (8) Cross Talk (CT):

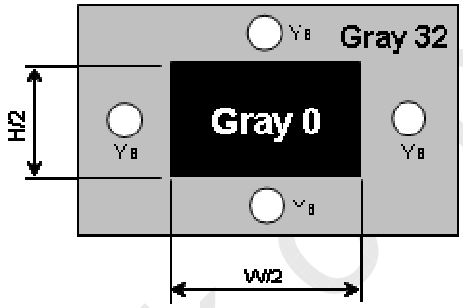
$CT = |Y_B - Y_A| / Y_A \times 100\%$

Where

Y_A=Luminance of measured location in left figure

Y_B=Luminance of measured location in right figure





Note (9) Definition of color gamut (C.G%):

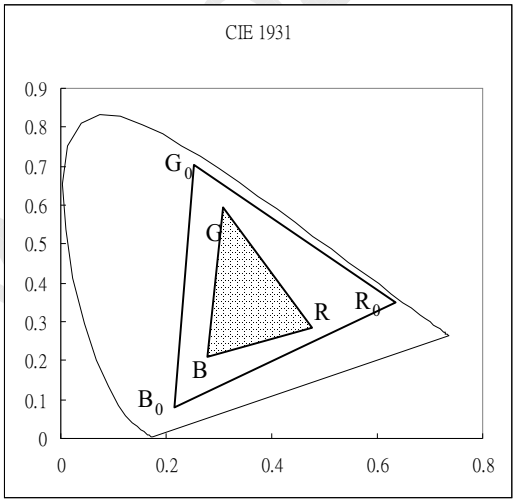
C.G%= Area (R, G, B) / Area (R_0, G_0, B_0,)* 100%

R_0, G_0, B_0: CIE1931 coordinates of red, green, and blue defined by NTSC.

R, G, B: CIE1931 coordinates of red, green, and blue in module at 63 gray level.

Area (R_0, G_0, B_0): Area of the triangle defined by coordinate R0, G0, B0.

Area(R, G, B): Area of the triangle defined by coordinate R, G, B



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6. RELIABILITY TEST ITEM

Test Item	Test Condition	Note
High Temperature Storage Test	70ºC, 240 hours	(1) (2)
Low Temperature Storage Test	-20ºC, 240 hours	
Thermal Shock Storage Test	-20ºC, 0.5hour←→70℃, 0.5hour; 100cycles, 1hour/cycle	
High Temperature Operation Test	60ºC, 240 hours	
Low Temperature Operation Test	-10ºC, 240 hours	
High Temperature & High Humidity Operation Test	60ºC, RH 90%, 240hours	
ESD Test (Operation)	150pF, 330Ω, 1sec/cycle Condition 1 : Contact Discharge, ±8KV Condition 2 : Air Discharge, ±15KV	(1)
Shock (Non-Operating)	220G, 2ms, half sine wave,1 time for each direction of ±X,±Y,±Z	(1)(3)
Vibration (Non-Operating)	1.5G / 10-500 Hz, Sine wave, 30 min/cycle, 1cycle for each X, Y, Z	(1)(3)

Note (1) criteria : Normal display image with no obvious non-uniformity and no line defect.

Note (2) Evaluation should be tested after storage at room temperature for more than two hour

Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

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7. PACKING

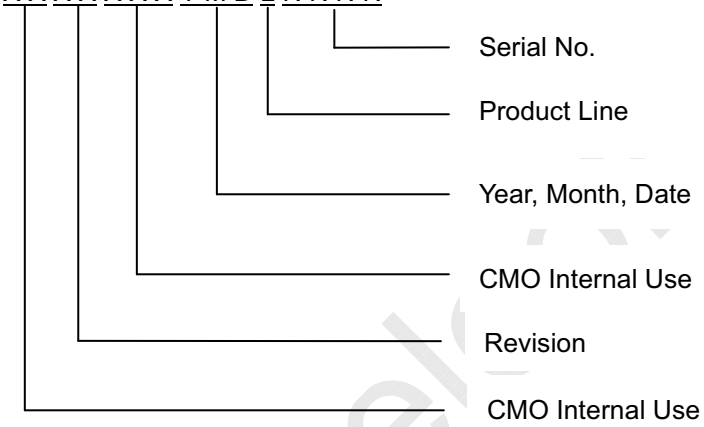
7.1 MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.

(a) Model Name: N101ICG – L11

(b) Revision: Rev. XX, for example: C1, C2 …etc.

(c) Serial ID: X X X X X X Y M D L N N N N



Serial ID includes the information as below:

(a) Manufactured Date: Year: 0~9, for 2010~2019

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U

(b) Revision Code: cover all the change

(c) Serial No.: Manufacturing sequence of product

(d) Product Line: 1 -> Line1, 2 -> Line 2, …etc.

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7.2 CARTON

Box Dimensions : 435(L)*350(W)*275(H)
Weight: Approx. 7.2kg(30 module .per. 1 box)

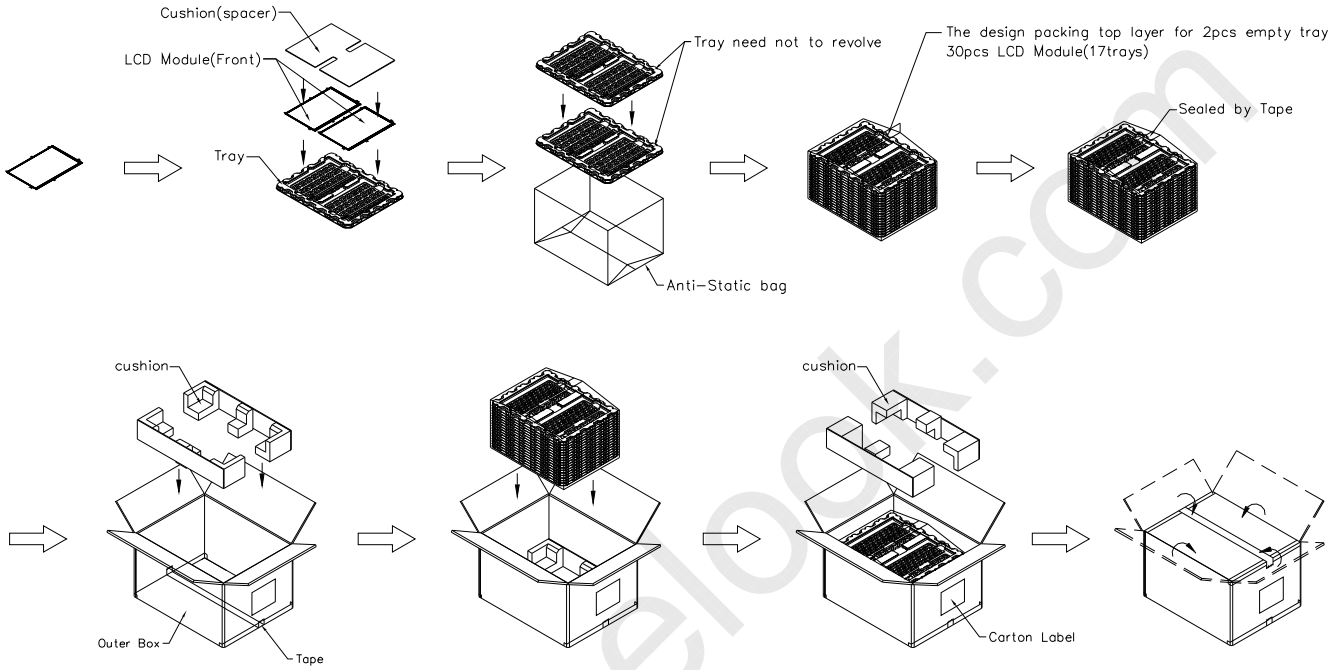

Figure. 7-1 Packing method

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7.3 PALLET

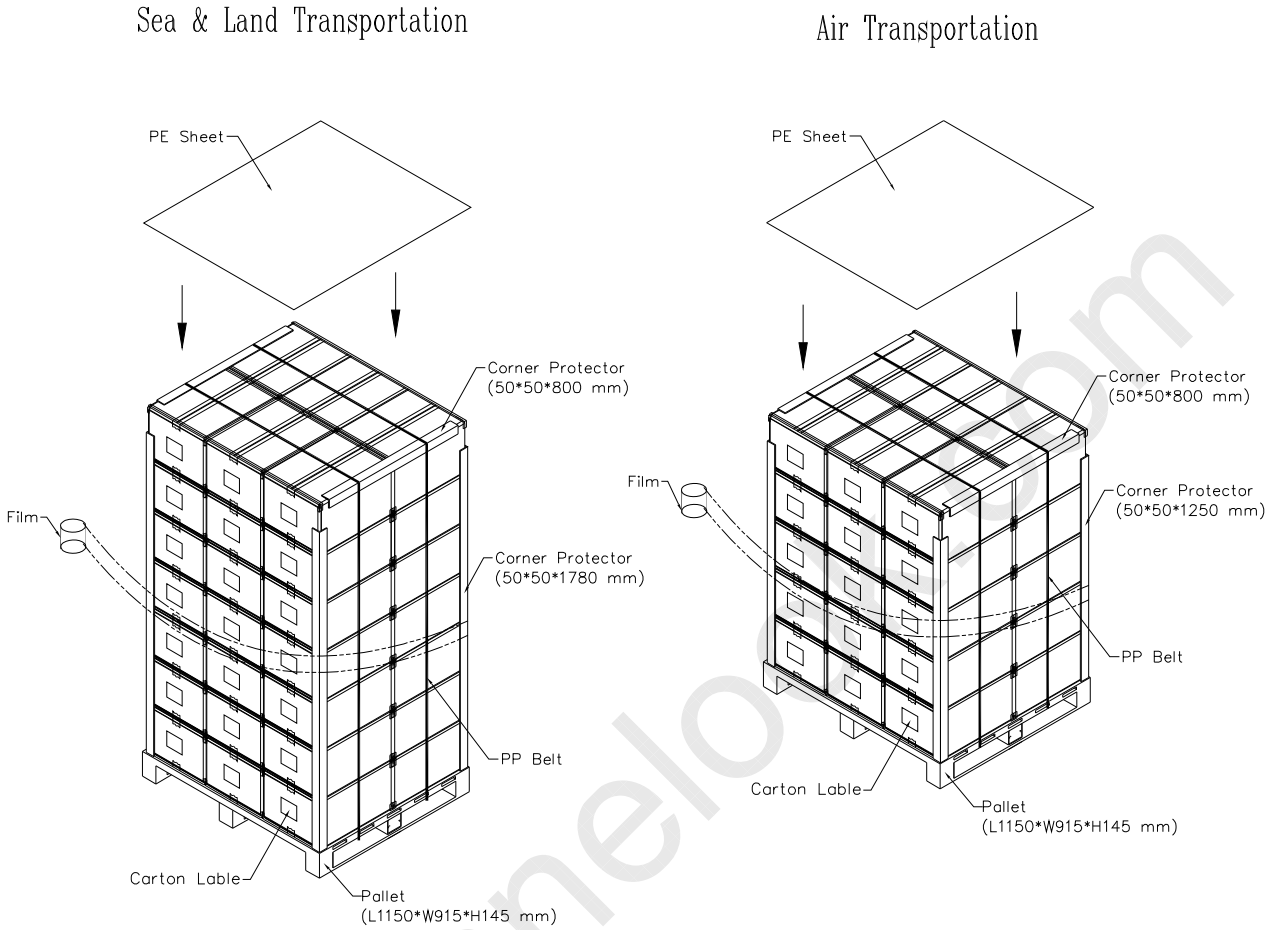

Figure. 7-2 Packing method

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7.4 Un-Packing

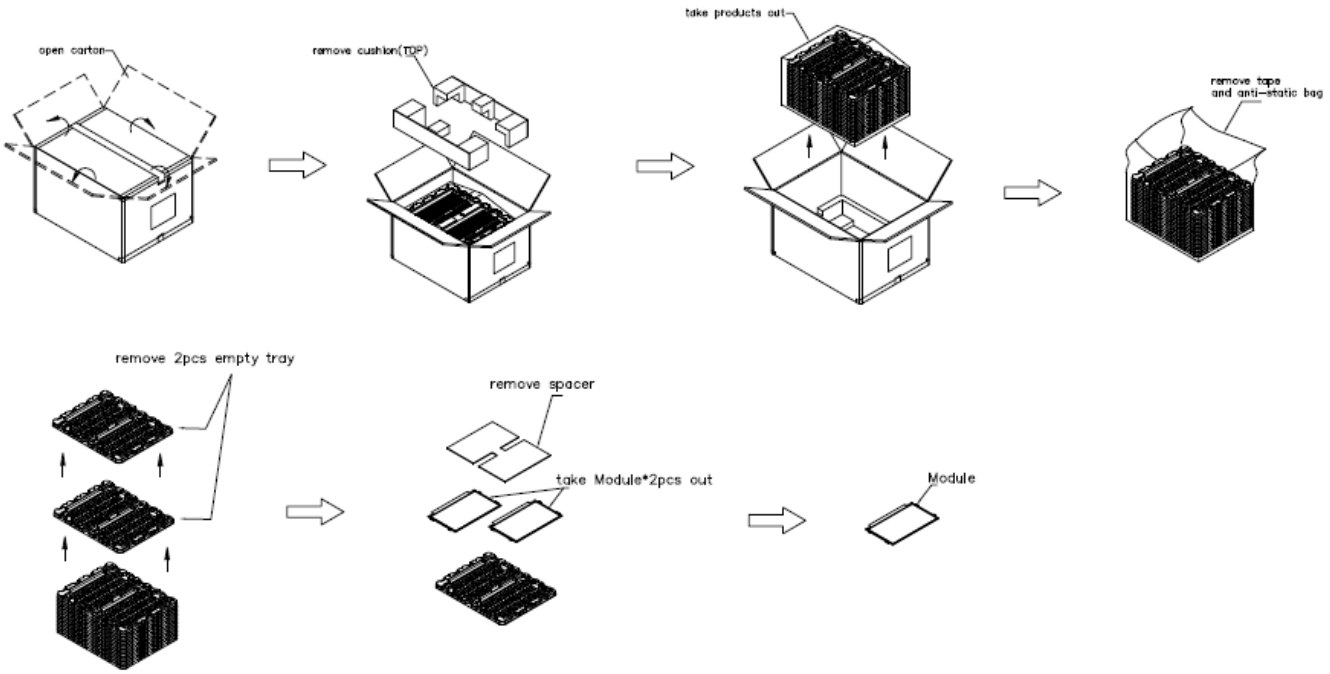

Figure. 7-3 Un-Packing method

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8. PRECAUTIONS

8.1 HANDLING PRECAUTIONS

(1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the module.

(10) Do not pull or fold the LED wire.

(11) Pins of I/F connector should not be touched directly with bare hands.

8.2 STORAGE PRECAUTIONS

(1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(3) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly, and the starting voltage of LED will be higher than the room temperature.

8.3 OPERATION PRECAUTIONS

(1) Do not pull the I/F connector in or out while the module is operating.

(2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.

(3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with converter. Do not disassemble the module or insert anything into the Backlight unit.

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Appendix. EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPDI standards.

Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	00	Header	00	00000000
1	01	Header	FF	11111111
2	02	Header	FF	11111111
3	03	Header	FF	11111111
4	04	Header	FF	11111111
5	05	Header	FF	11111111
6	06	Header	FF	11111111
7	07	Header	00	00000000
8	08	EISA ID manufacturer name ("CMN")	0D	00001101
9	09	EISA ID manufacturer name	AE	10101110
10	0A	ID product code (LSB)	41	01000001
11	0B	ID product code (MSB)	10	00010000
12	0C	ID S/N (fixed "0")	00	00000000
13	0D	ID S/N (fixed "0")	00	00000000
14	0E	ID S/N (fixed "0")	00	00000000
15	0F	ID S/N (fixed "0")	00	00000000
16	10	Week of manufacture (fixed week code)	1D	00011101
17	11	Year of manufacture (fixed year code)	17	00010111
18	12	EDID structure version ("1")	01	00000001
19	13	EDID revision ("3")	03	00000011
20	14	Video I/P definition ("Digital")	80	10000000
21	15	Active area horizontal (“21.696cm“)	16	00010110
22	16	Active area vertical (“13.56cm“)	0E	00001110
23	17	Display Gamma (Gamma = "2.2")	78	01111000
24	18	Feature support ("RGB Color")	0A	00001010
25	19	Rx1, Rx0, Ry1, Ry0, Gx1, Gx0, Gy1, Gy0	85	10000101
26	1A	Bx1, Bx0, By1, By0, Wx1, Wx0, Wy1, Wy0	BC	10111100
27	1B	Rx=0.592	97	10010111
28	1C	Ry=0.34	57	01010111
29	1D	Gx=0.31	4F	01001111
30	1E	Gy=0.579	94	10010100
31	1F	Bx=0.15	26	00100110
32	20	By=0.128	20	00100000
33	21	Wx=0.308	4E	01001110
34	22	Wy=0.324	53	01010011
35	23	Established timings 1	00	00000000
36	24	Established timings 2	00	00000000
37	25	Manufacturer's reserved timings	00	00000000
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 1	01	00000001
40	28	Standard timing ID # 2	01	00000001
41	29	Standard timing ID # 2	01	00000001

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42	2A	Standard timing ID # 3	01	00000001
43	2B	Standard timing ID # 3	01	00000001
44	2C	Standard timing ID # 4	01	00000001
45	2D	Standard timing ID # 4	01	00000001
46	2E	Standard timing ID # 5	01	00000001
47	2F	Standard timing ID # 5	01	00000001
48	30	Standard timing ID # 6	01	00000001
49	31	Standard timing ID # 6	01	00000001
50	32	Standard timing ID # 7	01	00000001
51	33	Standard timing ID # 7	01	00000001
52	34	Standard timing ID # 8	01	00000001
53	35	Standard timing ID # 8	01	00000001
54	36	Detailed timing description # 1 Pixel clock ("71.11MHz")	C7	11000111
55	37	# 1 Pixel clock (hex LSB first)	1B	00011011
56	38	# 1 H active ("1280")	00	00000000
57	39	# 1 H blank ("160")	A0	10100000
58	3A	# 1 H active : H blank	50	01010000
59	3B	# 1 V active ("800")	20	00100000
60	3C	# 1 V blank ("23")	17	00010111
61	3D	# 1 V active : V blank	30	00110000
62	3E	# 1 H sync offset ("48")	30	00110000
63	3F	# 1 H sync pulse width ("32")	20	00100000
64	40	# 1 V sync offset : V sync pulse width ("3 : 6")	36	00110110
65	41	# 1 H sync offset : H sync pulse width : V sync offset : V sync width	00	00000000
66	42	# 1 H image size (“216 mm“)	D8	11011000
67	43	# 1 V image size (“135 mm“)	87	10000111
68	44	# 1 H image size : V image size	00	00000000
69	45	# 1 H boarder ("0")	00	00000000
70	46	# 1 V boarder ("0")	00	00000000
71	47	# 1 Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives	18	00011000
72	48	Detailed timing description # 2	00	00000000
73	49	# 2 Flag	00	00000000
74	4A	# 2 Reserved	00	00000000
75	4B	# 2 ASCII string Model name	FE	11111110
76	4C	# 2 Flag	00	00000000
77	4D	# 2 Character of Model name ("N")	4E	01001110
78	4E	# 2 Character of Model name ("1")	31	00110001
79	4F	# 2 Character of Model name ("0")	30	00110000
80	50	# 2 Character of Model name ("1")	31	00110001
81	51	# 2 Character of Model name ("I")	49	01001001
82	52	# 2 Character of Model name ("C")	43	01000011
83	53	# 2 Character of Model name ("G")	47	01000111
84	54	# 2 Character of Model name ("-")	2D	00101101
85	55	# 2 Character of Model name ("L")	4C	01001100
86	56	# 2 Character of Model name ("1")	31	00110001
87	57	# 2 Character of Model name ("1")	31	00110001
88	58	# 2 New line character indicates end of ASCII string	0A	00001010

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89	59	# 2 Padding with "Blank" character	20	00100000
90	5A	Detailed timing description # 3	00	00000000
91	5B	# 3 Flag	00	00000000
92	5C	# 3 Reserved	00	00000000
93	5D	# 3 ASCII string Vendor	FE	11111110
94	5E	# 3 Flag	00	00000000
95	5F	# 3 Character of string ("C")	43	01000011
96	60	# 3 Character of string ("M")	4D	01001101
97	61	# 3 Character of string ("N")	4E	01001110
98	62	# 3 New line character indicates end of ASCII string	0A	00001010
99	63	# 3 Padding with "Blank" character	20	00100000
100	64	# 3 Padding with "Blank" character	20	00100000
101	65	# 3 Padding with "Blank" character	20	00100000
102	66	# 3 Padding with "Blank" character	20	00100000
103	67	# 3 Padding with "Blank" character	20	00100000
104	68	# 3 Padding with "Blank" character	20	00100000
105	69	# 3 Padding with "Blank" character	20	00100000
106	6A	# 3 Padding with "Blank" character	20	00100000
107	6B	# 3 Padding with "Blank" character	20	00100000
108	6C	Detailed timing description # 4	00	00000000
109	6D	# 4 Flag	00	00000000
110	6E	# 4 Reserved	00	00000000
111	6F	# 4 ASCII string Model Name	FE	11111110
112	70	# 4 Flag	00	00000000
113	71	# 4 Character of Model name ("N")	4E	01001110
114	72	# 4 Character of Model name ("1")	31	00110001
115	73	# 4 Character of Model name ("0")	30	00110000
116	74	# 4 Character of Model name ("1")	31	00110001
117	75	# 4 Character of Model name ("I")	49	01001001
118	76	# 4 Character of Model name ("C")	43	01000011
119	77	# 4 Character of Model name ("G")	47	01000111
120	78	# 4 Character of Model name ("-")	2D	00101101
121	79	# 4 Character of Model name ("L")	4C	01001100
122	7A	# 4 Character of Model name ("1")	31	00110001
123	7B	# 4 Character of Model name ("1")	31	00110001
124	7C	# 4 New line character indicates end of ASCII string	0A	00001010
125	7D	# 4 Padding with "Blank" character	20	00100000
126	7E	Extension flag	00	00000000
127	7F	Checksum	EB	11101011

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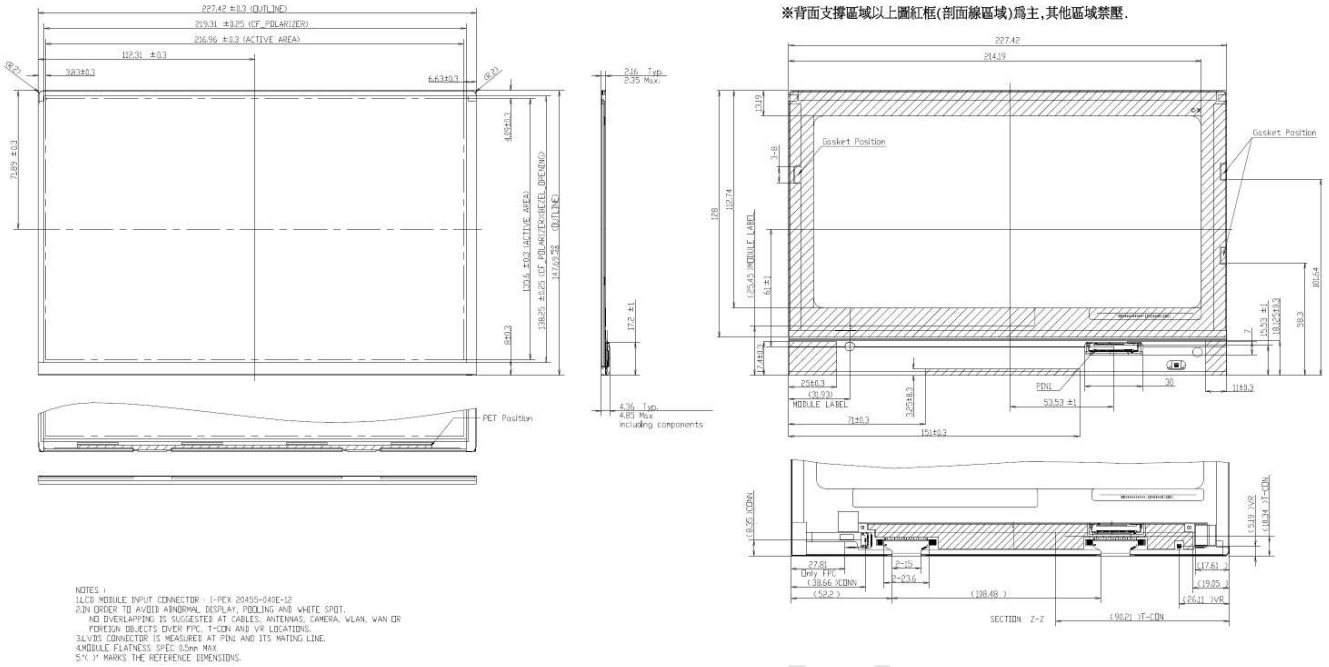
Appendix. OUTLINE DRAWING



NOTES :
1.LCD MODULE INPUT CONNECTOR : I-PEX 20455-040E-12
2.IN ORDER TO AVOID ABNORMAL DISPLAY, POOLING AND WHITE SPOT,
NO OVERLAPPING IS SUGGESTED AT CABLES, ANTENNAS, CAMERA, WLAN, WAN OR
FOREIGN OBJECTS OVER FPC, T-CON AND VR LOCATIONS.
3.LVDS CONNECTOR IS MEASURED AT PIN1 AND ITS MATING LINE.
4.MODULE FLATNESS SPEC: 0.5mm MAX.
5.'( )' MARKS THE REFERENCE DIMENSIONS.

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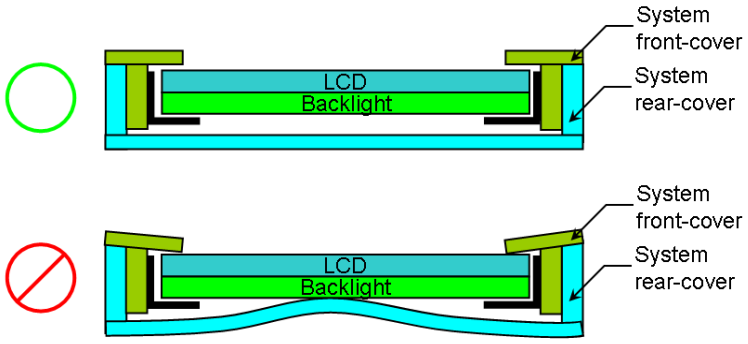
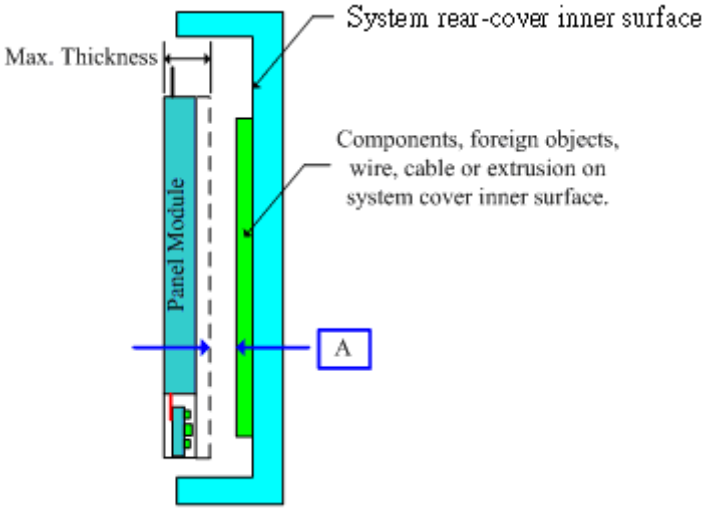
Appendix. SYSTEM COVER DESIGN GUIDANCE

0.	**Permanent deformation of system cover after reliability test**
	
Definition	System cover including front and rear cover may deform during reliability test. Permanent deformation of system front and rear cover after reliability test should not interfere with panel. Because it may cause issues such as pooling, abnormal display, white spot, and also cell crack.
1.	**Design gap A between panel & any components on system rear-cover**
	
Definition	Gap between panel's maximum thickness boundary & system's inner surface components such as wire, cable, extrusion is needed for preventing from backpack or pogo test fail. Because zero gap or interference may cause stress concentration. Issues such as pooling, abnormal display, white spot, and cell crack may occur. Flatness of panel and system rear-cover should be taken into account for gap design.
2	**Design gap B1 & B2 between panel & protrusions**

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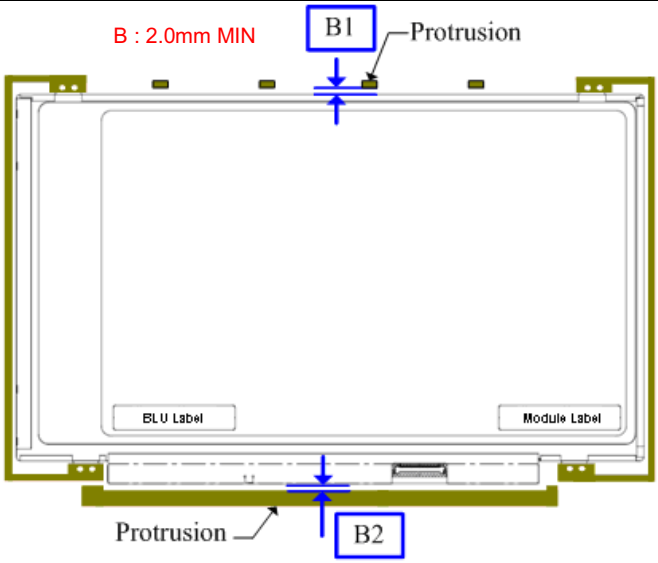
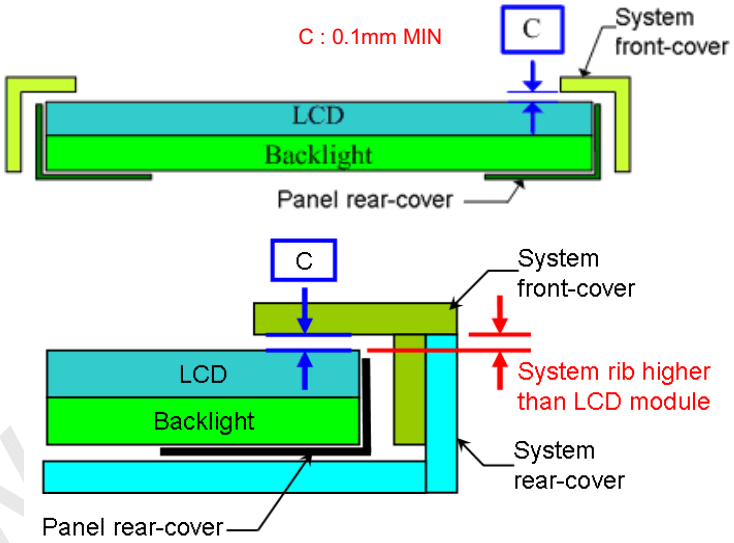
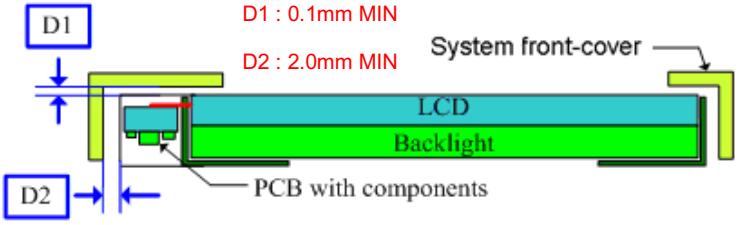


Definition	Gap between panel & protrusions is needed to prevent shock test failure. Because protrusions with small gap may hit panel during the test. Issue such as cell crack, abnormal display may occur.
3	**Design gap C between system front-cover & panel surface.**



Definition	Gap between system front-cover & panel surface is needed to prevent pooling or glass broken. Zero gap or interference such as burr and warpage from mold frame may cause pooling issue near system font-cover opening edge. This phenomenon is obvious during swing test, hinge test, knock test, or during pooling inspection procedure. To remain sufficient gap, design with system rib higher than maximum panel thickness is recommended.
4	**Design gap D1 & D2 between system front-cover & PCB Assembly.**



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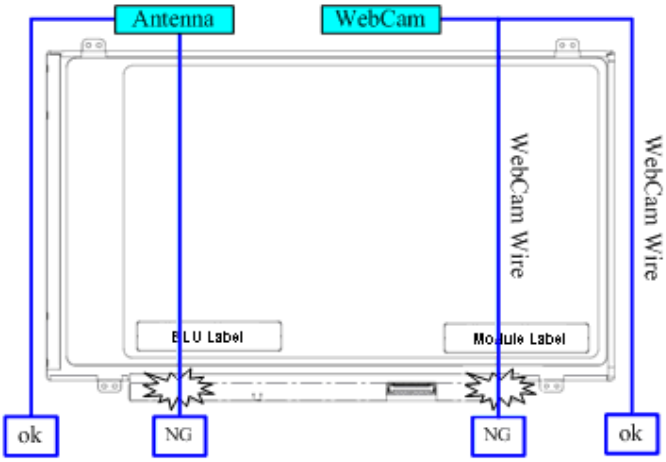
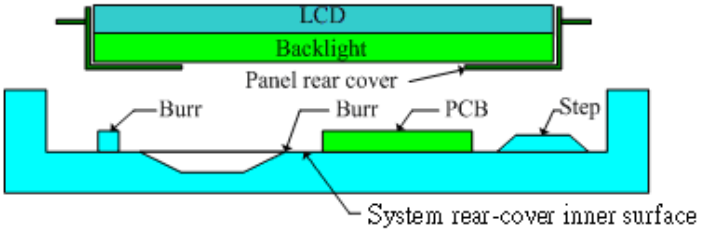
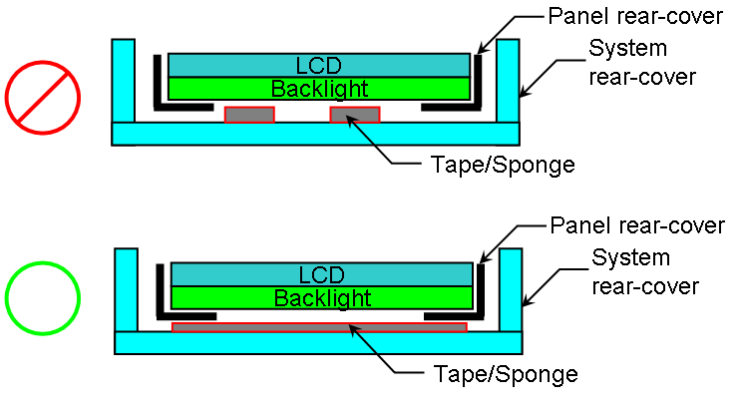
Definition	Same as point 2 and 3, but focus on PCBA side.
5	**Interference examination of antenna cable and WebCam wire**
	
Definition	Antenna cable or WebCam wire should not overlap with panel outline. Because issue such as abnormal display & white spot after backpack test, hinge test, twist test or pogo test may occur.
6	**System rear-cover inner surface examination**
	
Definition	Burr at logo edge, steps, protrusions or PCB board may cause stress concentration. White spot or glass broken issue may occur during reliability test.
7	**Tape/sponge design on system inner surface**
	
Definition	To prevent abnormal display & white spot after scuffing test, hinge test, pogo test, backpack test, tape/sponge should be well covered under panel rear-cover. Because tape/sponge in separate location may act as pressure concentration location.

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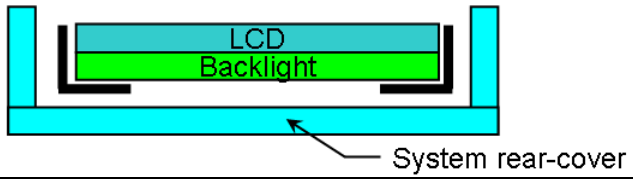
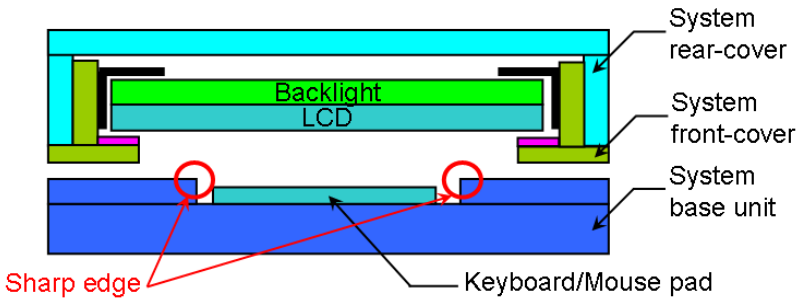
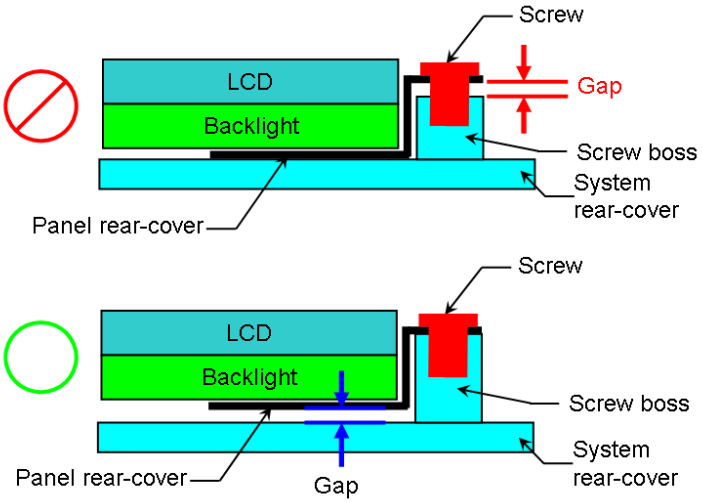
8	**Material used for system rear-cover**
	
Definition	System rear-cover material with high rigidity is needed to resist deformation during scuffing test, hinge test, pogo test, or backpack test. Abnormal display, white spot, pooling issue may occur if low rigidity material is used. Pooling issue may occur because screw's boss positioning for module's bracket are deformed during open-close test. Solid structure design of system rear-cover may also influence the rigidity of system rear-cover. The deformation of system rear-cover should not caused interference.
9	**System base unit design near keyboard and mouse pad**
	
Definition	To prevent abnormal display & white spot after scuffing test, hinge test, pogo test, backpack test, sharp edge design in keyboard surface may damage panel during the test. We suggest to use slope edge design, or to reduce the thickness difference of keyboard/mouse pad from the nearby surface.
10	**Screw boss height design**
	
Definition	Screw boss height should be designed with respect to the height of bracket bottom surface to panel bottom surface + flatness change of panel itself. Because gap will exist between screw boss and bracket, if the screw boss height is smaller. As result while fastening screw, bracket will deformed and pooling issue may occur.
11	**Assembly SOP examination for system front-cover with Hook design**

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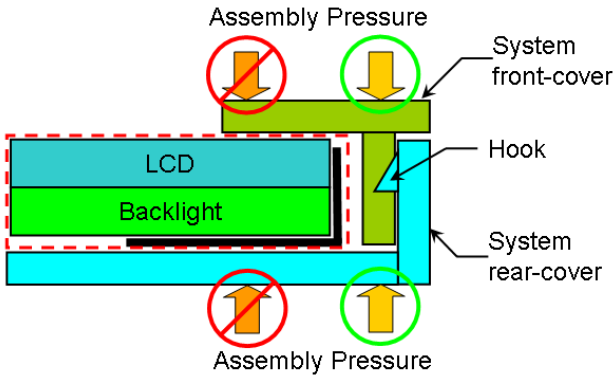
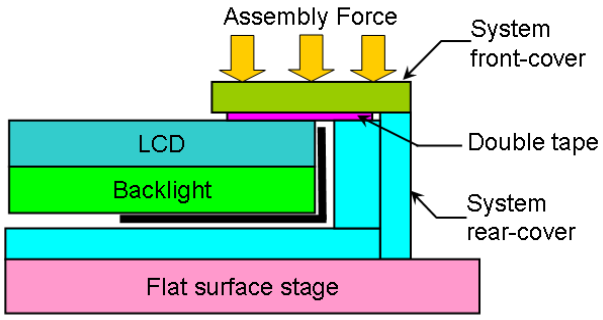


Definition	To prevent panel crack during system front-cover assembly process with hook design, it is not recommended to press panel or any location that related directly to the panel.
12	**Assembly SOP examination for system front-cover with Double tape design**



Definition	To prevent panel crack during system front-cover assembly process with double tape design, it is only allowed to give slight pressure (MAX 3 Kgf/50mm2) with large contact area. This can help to distribute the stress and prevent stress concentration. We also suggest putting the system on a flat surface stage to prevent unequal stress distribution during the assembly.

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